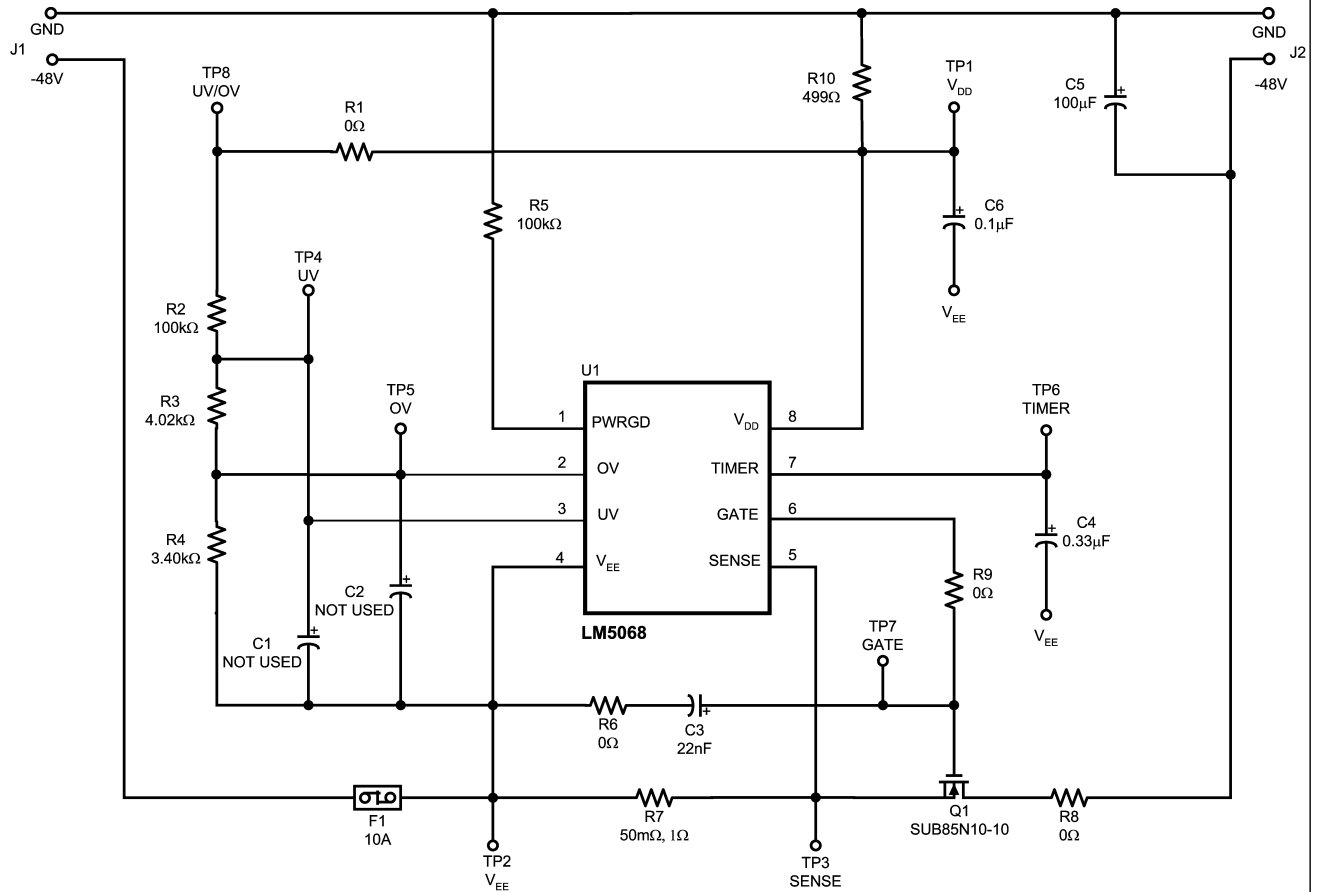


Theory Of Operation (Continued)



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FIGURE 2.

The apparatus required to test the evaluation board is as follows:

1. 100V/ 5A DC power supply
2. 2 or 4 channel analog or digital storage oscilloscope
3. Two RMS voltmeters (DVM) with floating inputs

Care must be exercised while operating at high input voltages.

Operational Description of the Evaluation Board

The operation of LM5068 hot-swap controller embedded on a plug-in board, can be categorized into three parts, namely,

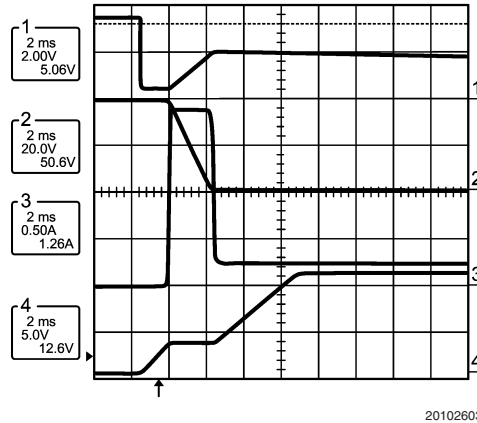
- Start-up and inrush current limiting
- Auto retry following the detection of a fault

- Load disconnect and power limiting during fault
- Each of these phases is explained briefly as follows.

Start-up and Inrush Current Limit

Whenever a circuit card with large electrolytic capacitors is inserted into a live backplane, large inrush currents will occur. These surge currents can cause the backplane voltage to drop, which can reset or otherwise interfere with adjacent boards. The current surges can also affect connector pins, burn out PCB traces and can interfere with data by generating EMI. The LM5068 actively limits inrush currents, which limits load voltage slew rate ($\Delta V/\Delta t$). The LM5068 has active current limiting threshold of 100mV, and an R_{SENSE} equal to 50mΩ, therefore the maximum current is limited to 2.0A (refer to *Figure 3* below).

Operational Description of the Evaluation Board (Continued)



CH1: Timer Pin Voltage
 CH2: Voltage Across MOSFET Switch
 CH3: Load Current
 CH4: Gate Voltage

FIGURE 3. Start-Up Characteristics

Auto Retry During Faults:

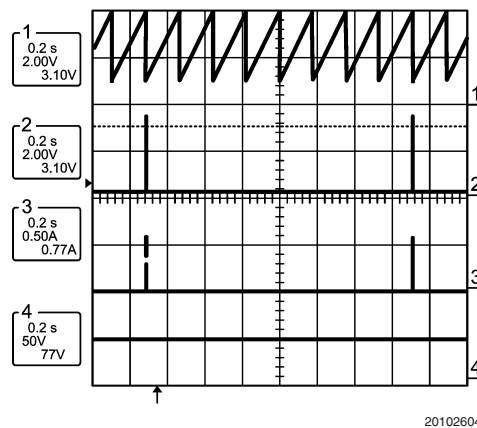
If the fault conditions persist long enough for TIMER pin to charge C_T to 4V, the LM5068 latches off (LM5068-1, -3) or switches off and initiates the re-try timer (LM5068-2, -4).

The LM5068-1 and LM5068-3 remains off until the controller is reset by either temporarily pulling the UV pin low, pulling the TIMER pin below 1 volt, or decreasing the input voltage below the internal V_{DD} under-voltage lockout (UVLO) threshold.

The LM5068-2 and LM5068-4 respond to a fault condition by pulling the GATE and TIMER pins low and then initiating a

timer sequence for automatic re-try. The re-try timer sequence begins with C_T capacitor being charged slowly to 4V with a 6 μ A current source and then discharged quickly to 1V with a 30mA discharge current. After eight charge/discharge cycles the GATE pin is released and charged with a 60 μ A current source. If the fault condition persists, the LM5068 will again turn off the MOSFET and another 8-cycle fault timer sequence will begin.

The Evaluation board is provided with a LM5068-2, which features the auto retry following a fault detection (refer to Figure 4).



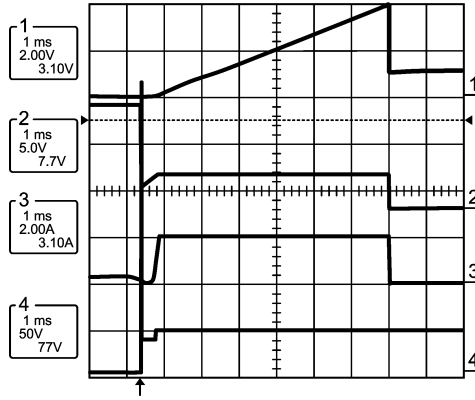
CH1: Timer Pin Voltage
 CH2: Gate Pin Voltage
 CH3: Current Through MOSFET
 CH4: Voltage Across MOSFET

FIGURE 4. Auto Retry Feature after Fault Detection

Load Disconnect and Power Limit During Catastrophic Faults

During catastrophic faults like short-circuit on the output when the series MOSFET is fully enhanced, high inrush currents are still possible. To prevent these high surge currents, the LM5068 has a fast current limit threshold of 200mV. Fast Discharge Current (FDC) responds to fast ris-

ing over-loads such as short circuit faults. During a short circuit event the fast rising current may overshoot past the ACL (active current limit) threshold of 100mV due to the finite response time of the ACL loop. If the SENSE voltage reaches 200mV a fast discharge comparator quickly pulls GATE pin low. The rapid response of the FDC circuit assures a fast and safe transition to the ACL mode.



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CH1: Timer Pin Voltage
 CH2: Gate Pin Voltage
 CH3: Current Through MOSFET
 CH4: Voltage Across MOSFET

FIGURE 5. Fast Response Circuit Breaker during Output Short Circuit

The LM5068 circuit breaker action filters low duty cycle over-load conditions to avoid declaring a fault during short duration load transients. The timer charges capacitor C_T with 240 μ A when the SENSE voltage is greater than 50mV. When the SENSE pin voltage falls below 50mV, a 6 μ A current discharges the TIMER capacitor. Repetitive over-current faults with duty cycle greater than 2.5% will eventually charge CT and trip the fault timer. This feature protects the pass MOSFET, which has a fast heating and slow cooling characteristic.

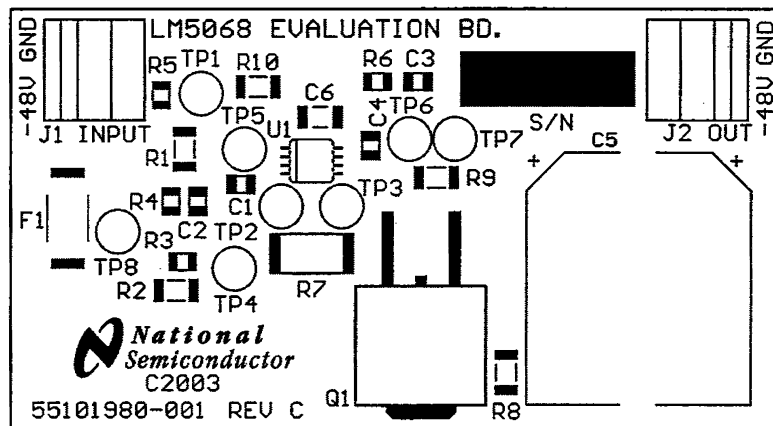
Conclusion

This application note explains the apparatus and method needed to operate the LM5068 evaluation board in a typical environment. Typical operating modes have been explained with reference to the evaluation board.

Component List

PART	VALUE	PACKAGE	DESCRIPTION	PART NUMBER
C1	NOT USED			
C2	NOT USED			
C3	0.022 μ F / 50V	C0805	CAPACITOR, CERAMIC, KEMET	C0805C223K5RAC
C4	0.33 μ F / 50V	C0805	CAPACITOR, CERAMIC, KEMET	C0805C334K5RAC
C5	100 μ F / 100V		CAPACITOR, ALUMINIUM ELECTROLYTIC, SURFACE MOUNT, PANASONIC	EEV-FK2A101M
C6	0.1 μ F / 100V	C1206	CAPACITOR, CERAMIC, TDK	C3216X7R2A104KT
F1	10A FUSE	SMD_FUSE	COOPER BUSSMAN FAST ACTING FUSE TRON	TR/SFT-10 (Digikey # 283-2439-2-ND)
J1	PCB terminal Blocks/ 10A		MOUSER TERMINAL BLOCKS	651-1727010
J2	PCB terminal Blocks/ 10A		MOUSER TERMINAL BLOCKS	651-1727010
Q1	100V / 60A	N-Channel Power MOSFET, TO263	VISHAY	SUB85N10-10
R1	0	R1206	SMD RESISTOR, 1% TOL	CRCW12060000F
R2	100k	R1206	SMD RESISTOR, 1% TOL	CRCW12061003F
R3	4.02k	R0805	SMD RESISTOR, 1% TOL	CRCW08054020F
R4	3.40k	R0805	SMD RESISTOR, 1% TOL	CRCW08053401F
R5	100k	R0805	SMD RESISTOR, 1% TOL	CRCW08051003F
R6	0	R0805	SMD RESISTOR, 1% TOL	CRCW08050000F
R7	50m	R2512	SMD RESISTOR, 1% TOL	WSL-2512 .050F
R8	0	R1206	SMD RESISTOR, 1% TOL	CRCW12060000F
R9	0	R1206	SMD RESISTOR, 1% TOL	CRCW12060000F
R10	499	R1206	SMD RESISTOR, 1% TOL	CRCW1206499RF
U1	LM5068	MSOP-8	National Semiconductor	LM5068-2

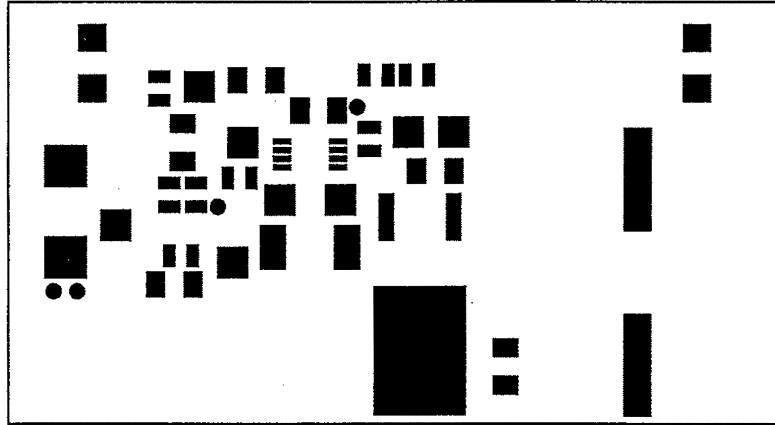
PCB Layouts



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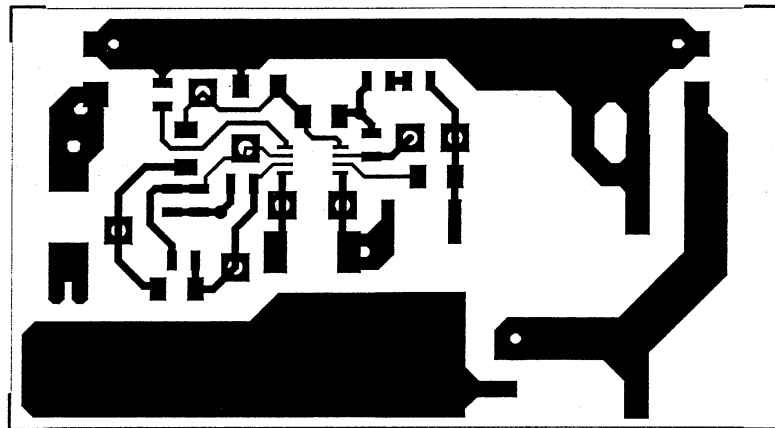
Silkscreen Layer as viewed from Top

PCB Layouts (Continued)



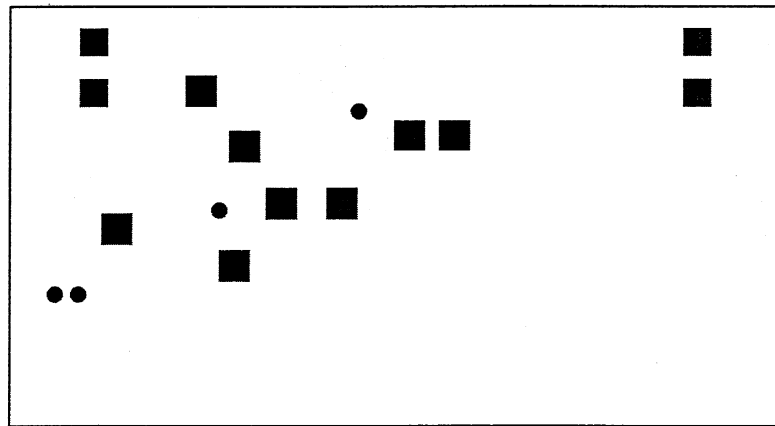
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Top Side Soldermask as viewed from Top



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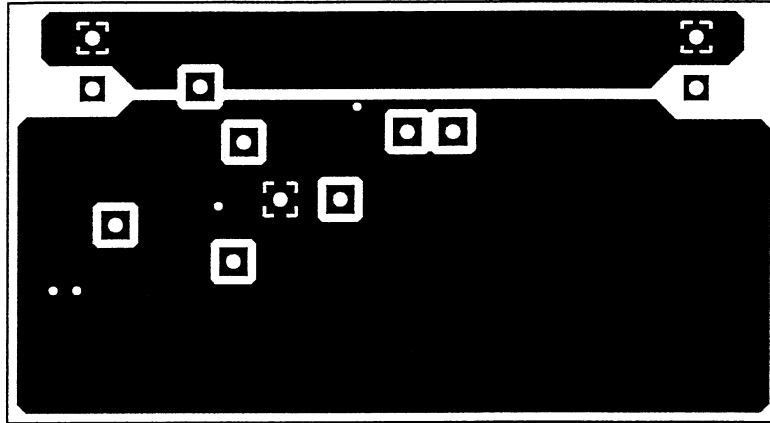
Top (Component) Layer as viewed from Top



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Bottom Side Soldermask as viewed from Top

PCB Layouts (Continued)



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Bottom (Solder) Layer as viewed from Top

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